



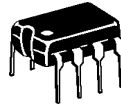
MC34063A DC -TO- DC CONVERTER CONTROL CIRCUITS

DESCRIPTION

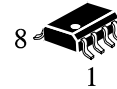
The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

FEATURES

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

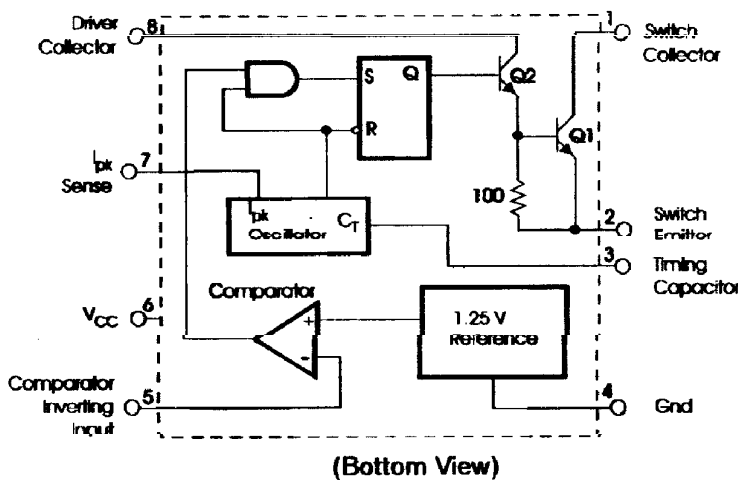


CDSUFFIX
PLASTIC PACKAGE
DIP-8

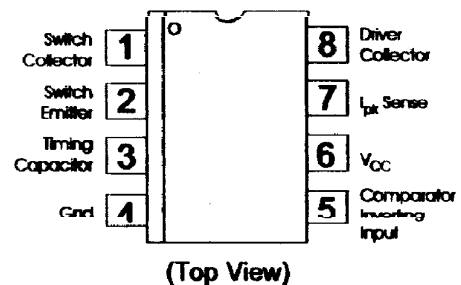


CSSUFFIX
PLASTIC PACKAGE
SOP-8

SCHEMATIC DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{PIN1} = 40 V$)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



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ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0\text{ V}$, $T_A = T_{low}$ to T_{high} , unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{pin5} = 0\text{V}$, $C_T = 1.0\text{ nF}$, $T_A = 25^\circ\text{C}$)	f_{osc}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0\text{V to } 40\text{V}$, $T_A = 25^\circ\text{C}$)	I_{chg}	24	35	42	μA
Discharge Current ($V_{CC} = 5.0\text{V to } 40\text{V}$, $T_A = 25^\circ\text{C}$)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC} , $T_A = 25^\circ\text{C}$)	I_{dischg}/I_{chg}	5.2	6.5	7.5	—
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, $T_A = 25^\circ\text{C}$)	$V_{ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (NOTE 2)					
Saturation Voltage, Darlington Connection ($I_{sw} = 1.0\text{ A}$, Pins 1, 8 connected)	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage, Darlington Connection ($I_{sw} = 1.0\text{ A}$, $R_{pin8} = 82\Omega$ to V_{CC} , Forced $\beta \approx 20$)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain ($I_{sw} = 1.0\text{ A}$, $V_{CE} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	h_{FE}	50	75	—	—
Collector Off-State Current ($V_{CE} = 40\text{ V}$)	$I_{C(off)}$	—	40	100	μA
COMPARATOR					
Threshold Voltage ($I_A = 25^\circ\text{C}$) ($T_A = T_{low}$ to T_{high})	V_{th}	1.225 1.21	1.25 —	1.275 1.29	V
Threshold Voltage Line Regulation ($V_{CC} = 3.0\text{ V to } 40\text{ V}$)	Reg_{line}	—	1.4	5.0	mV
Input Bias Current ($V_{in} = 0\text{ V}$)	I_{IB}	—	-20	-400	nA
TOTAL DEVICE					
Supply Current ($V_{CC} = 5.0\text{ V to } 40\text{ V}$, $C_T = 1.0\text{ nF}$, Pin 7 = V_{CC} , $V_{pin5} > V_{th}$, Pin 2 = Gnd, remaining pins open)	I_{CC}	—	—	4.0	mA

NOTES :

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.



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Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor

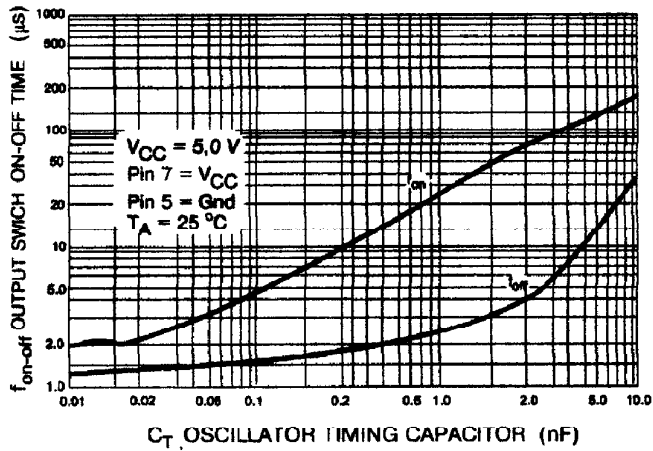


Figure 2. Timing Capacitor Waveform

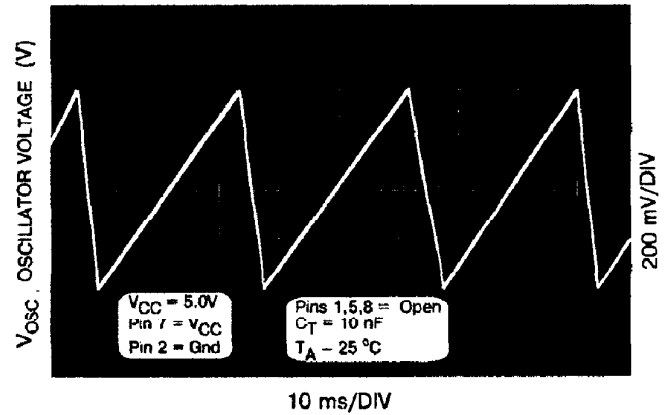


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

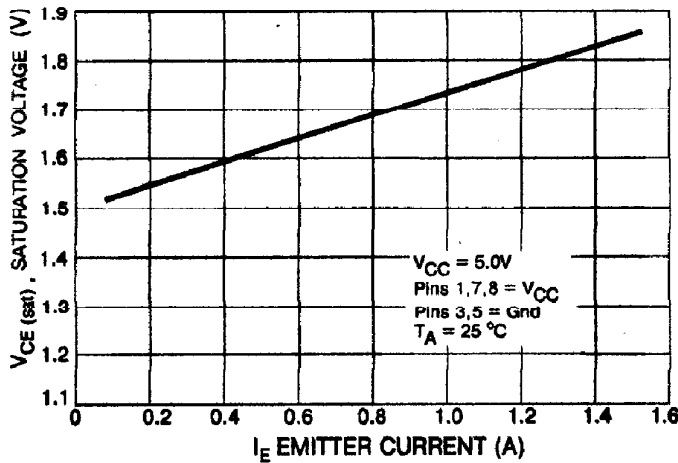


Figure 4. Common Emitter Configuration Output Switch Voltage versus Collector Current

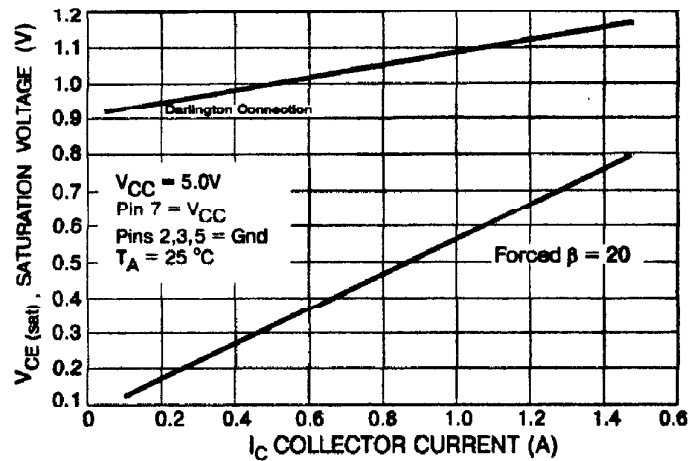


Figure 5. Current Limit Sense Voltage versus Temperature

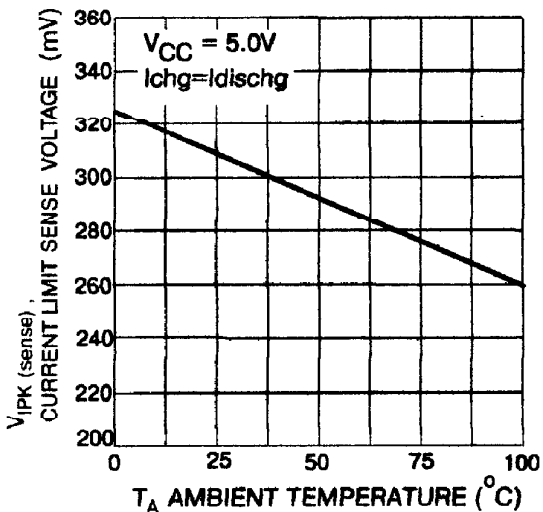
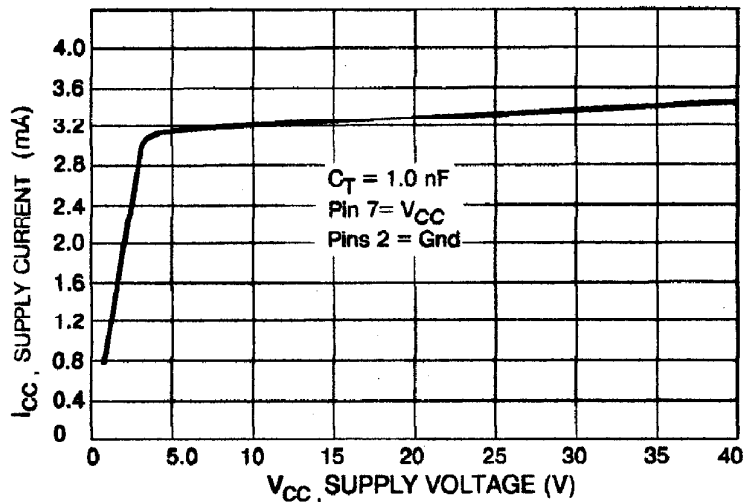


Figure 6. Standby Supply Current versus Supply Voltage





APPLICATION INFORMATION

Figure 1. Step-Up Converter

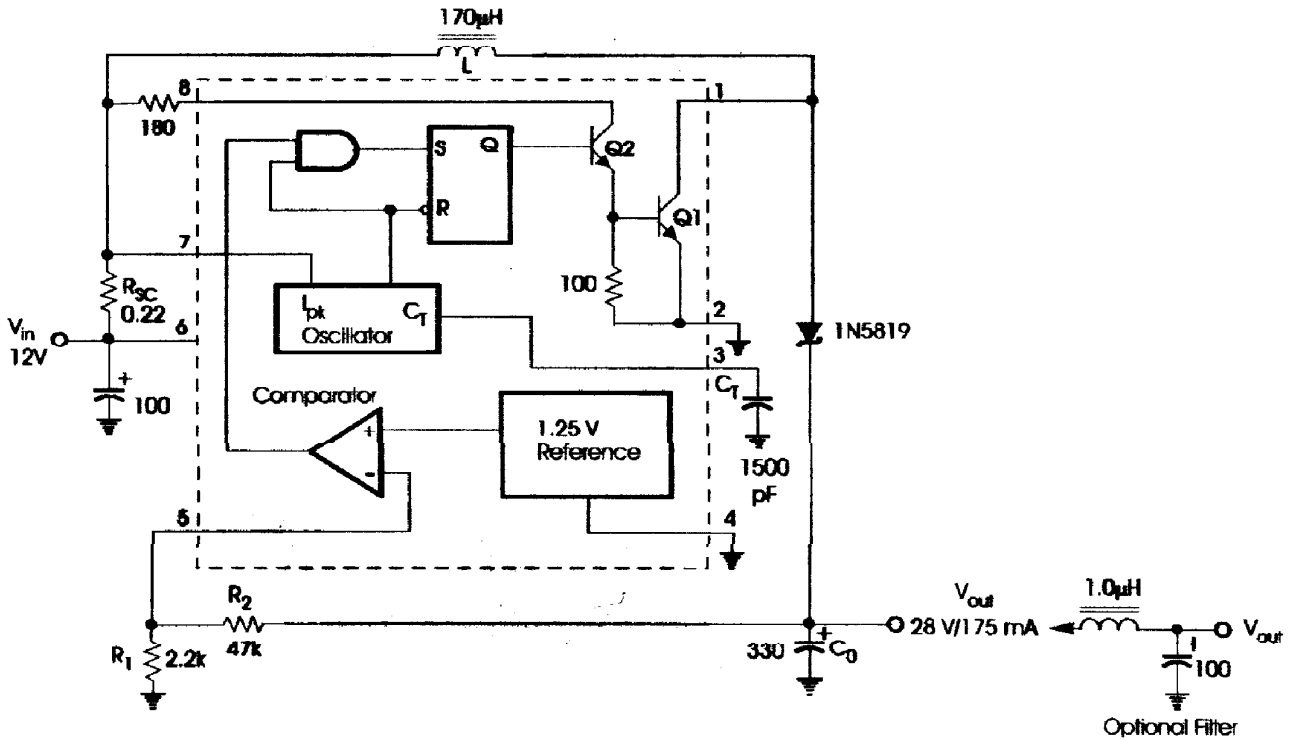
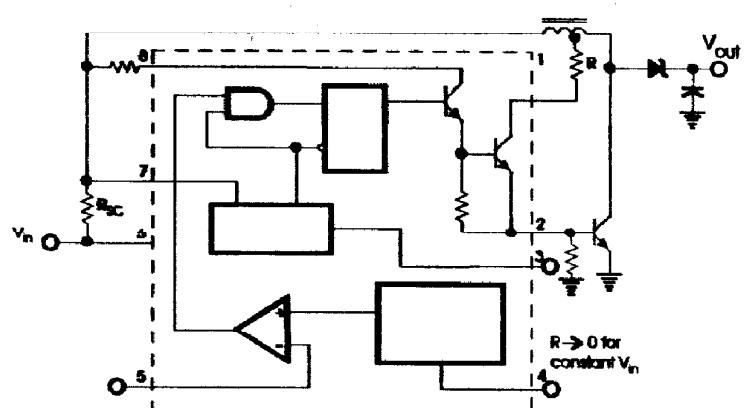
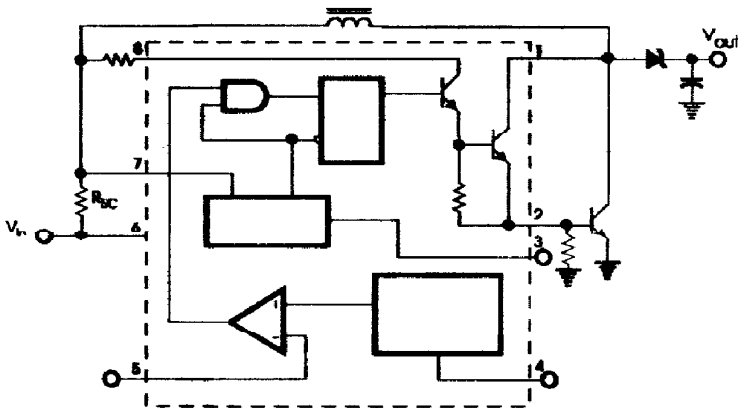


Figure 2. External Current Boost Connections for I_C Peak Greater than 1.5 A

2a. External NPN Switch

2b. External NPN Saturated Switch





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Figure 3. Step-Down Converter

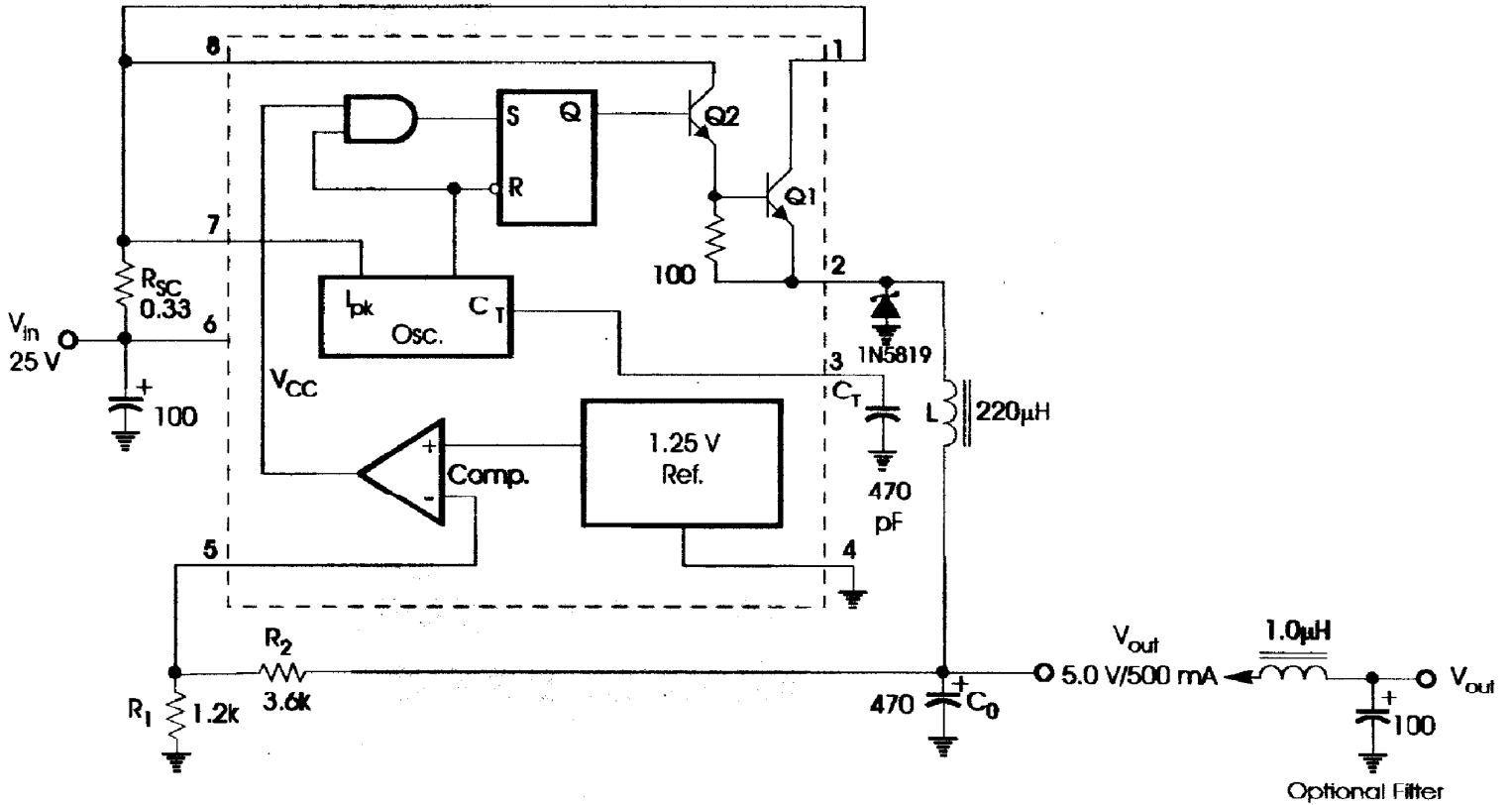
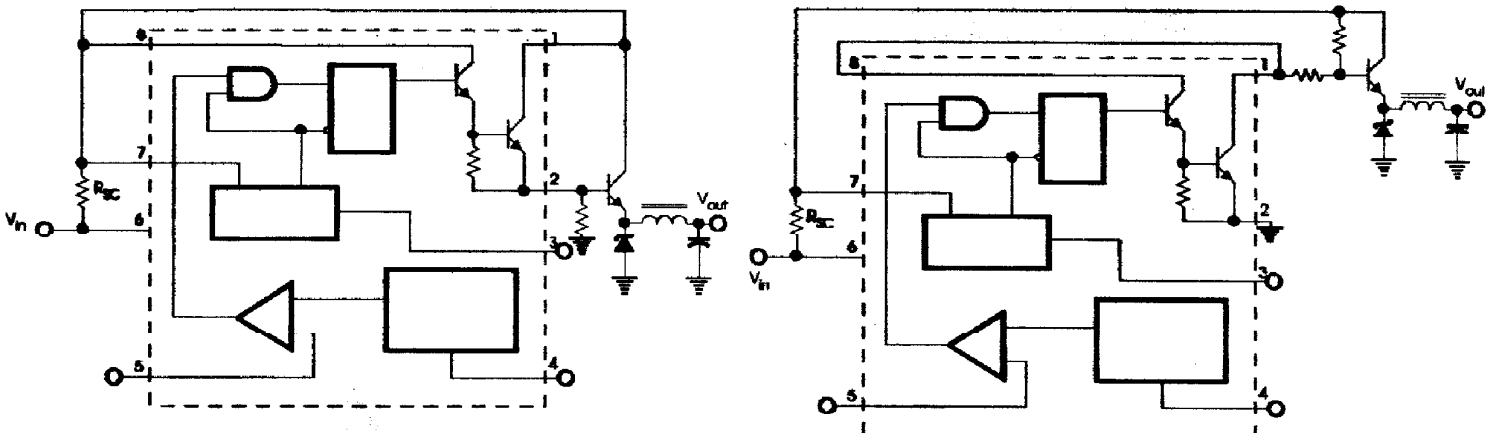


Figure 4. External Current Boost Connections for I_c Peak Greater than 1.5 A

4a. External NPN Switch

4b. External NPN Switch





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Figure 5. Voltage Inverting Converter

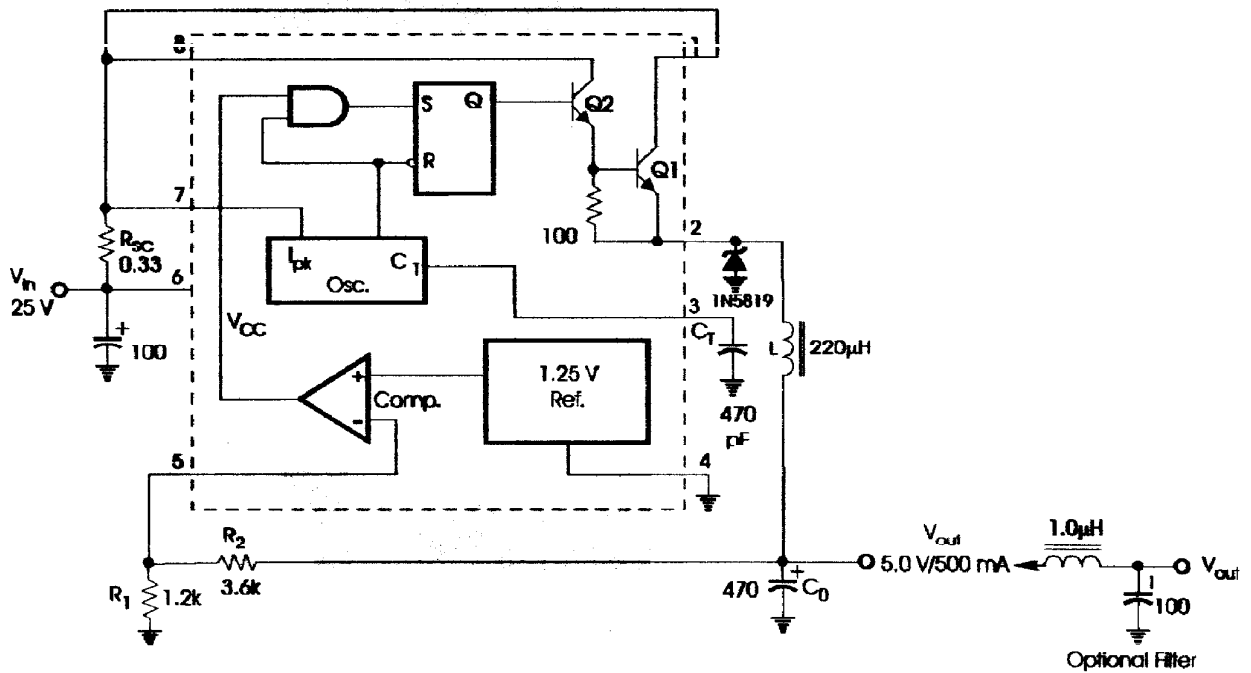
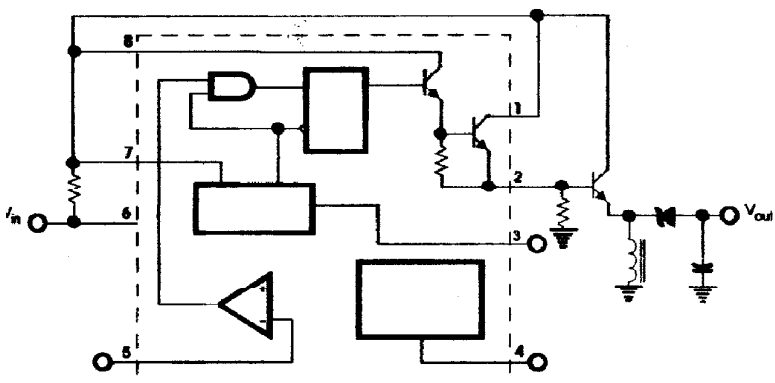
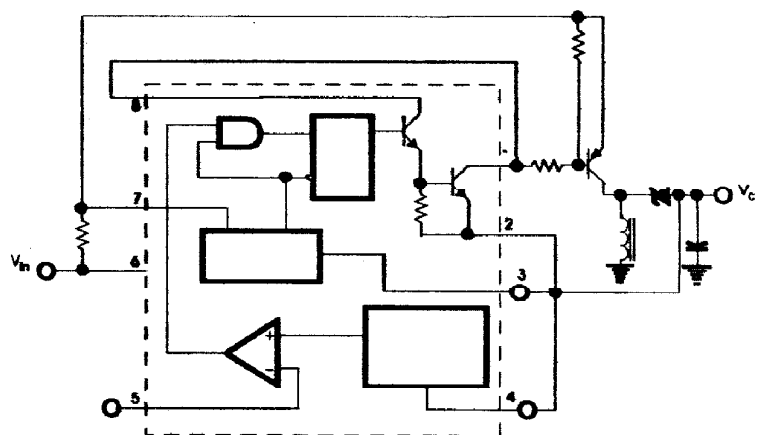


Figure 6. External Current Boost Connections for I_C Peak Greater than 1.5 A

6a. External NPN Switch



6b. External PNP Saturated Switch





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Figure 7. Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk}(switch)$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$0.3/I_{pk}(switch)$	$0.3/I_{pk}(switch)$	$0.3/I_{pk}(switch)$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk}(switch)} \right) = t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk}(switch)} \right) = t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk}(switch)} \right) = t_{on(max)}$
C_o	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk}(switch) (t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

TERMS AND DEFINITIONS

V_{sat} - Saturation voltage of the output switch.

V_F - Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

I_{out} - Desired output current.

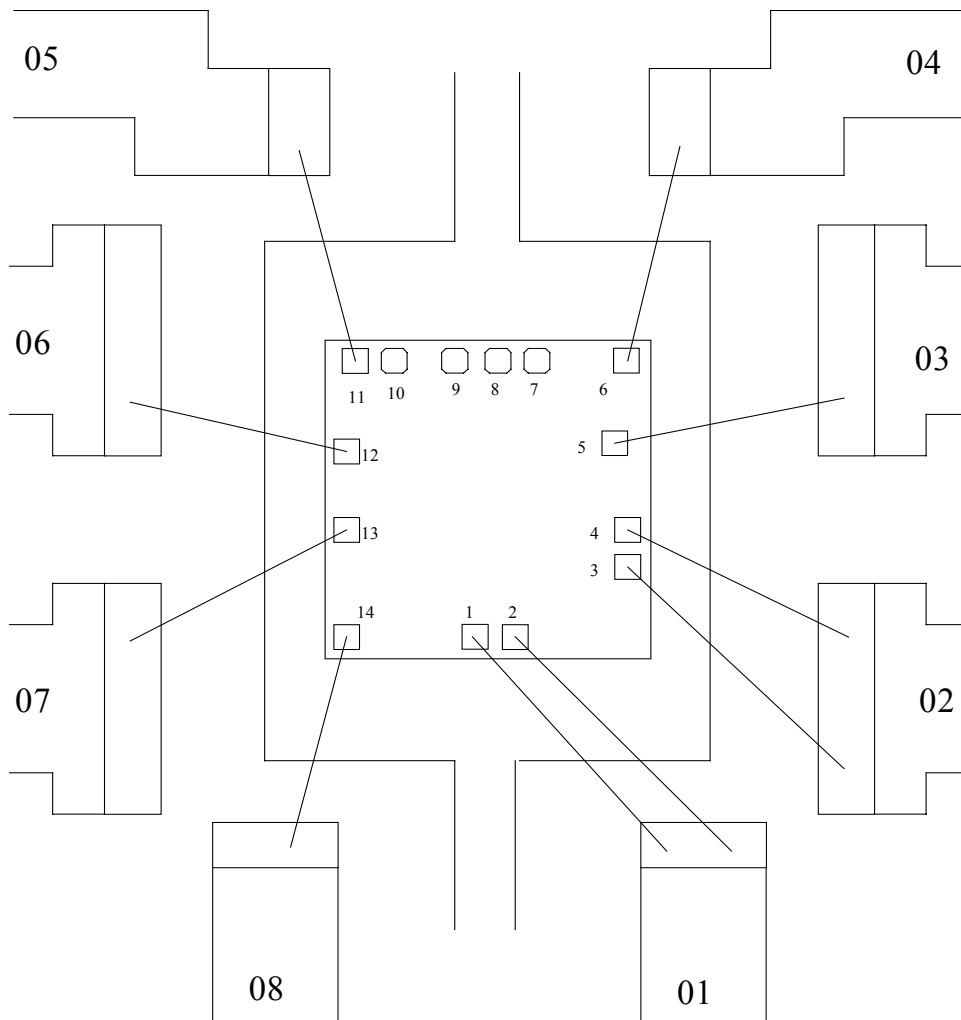
f_{min} - Minimum desired output switching frequency at the selected values of V_{in} and I_o .

$V_{ripple(p-p)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.



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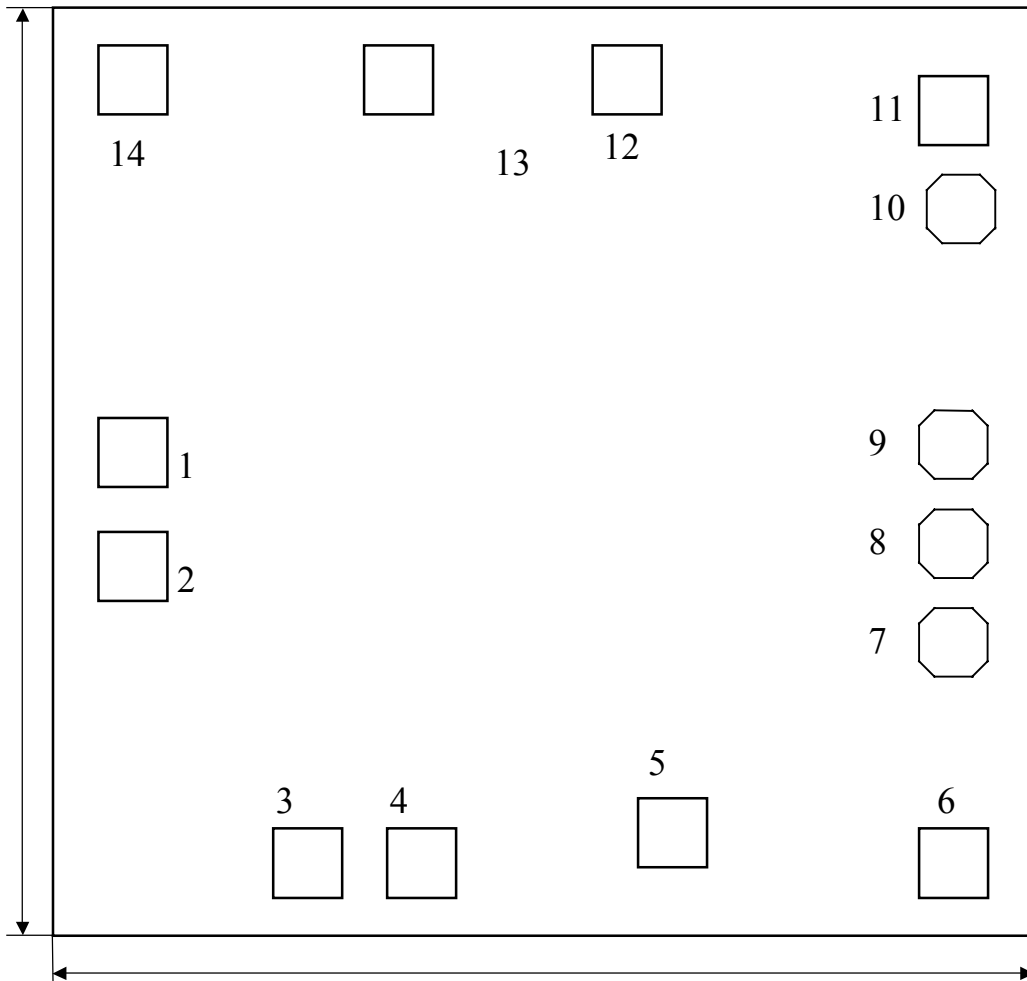
Pad Location MC 34063A



Bonding diagram of 34063A



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34063A

Die size $X_r=1.83\text{mm}$, $Y_r=1.82\text{mm}$ (pad size $120 \times 120 \mu\text{m}^2$)

No. of pad	Xmin	Xmax	Ymin	Ymax
1	83	203	847	967
2	83	203	671	791
3	683	803	85	205
4	853	973	85	205
5	1121	1241	145	265
6	1630	1750	85	205
7*	1602	1702	813	913
8*	1602	1702	961	1061
9*	1602	1702	1109	1209
10*	1582	1697	1283	1383
11	1577	1697	1485	1605
12	943	1063	1620	1740
13	624	744	1620	1740
14	80	200	1615	1735

***-technological pads, not for bonding**