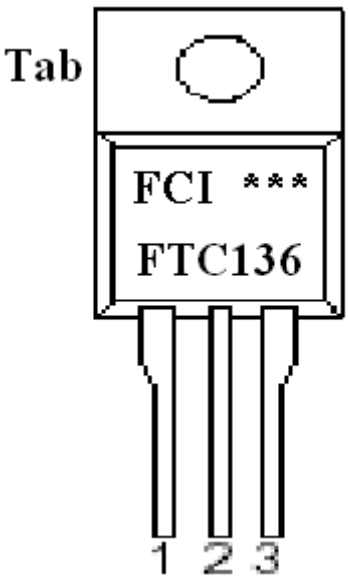
4A 600V BIDIRECTIONAL TRIACS



TO-220AB

Description:

Passivated triacs in a Plastic envelop, intended for use in applications requiring high bidirectional transient and blocking voltage capability and **high thermal cycling performance. Typical applications imclude motor control, industrial and** domestic lighting, heating and static switching

FTC131

V_{DRM} 600V

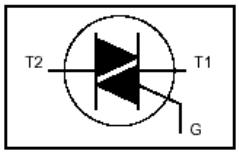
$I_{T(RMS)}$ 4A

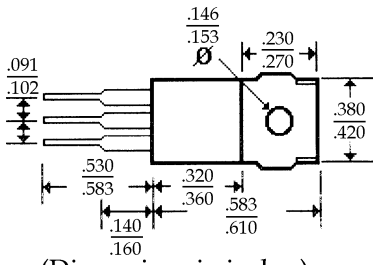
I_{TSM} 25A

PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

SYMBOL





(Dimensions in inches)

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C	-	4	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge			
		t = 20 ms	-	25	A
		t = 16.7 ms	-	27	A
I^2t	I^2t for fusing	t = 10 ms	-	3.1	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 6 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs			
		T2+ G+	-	50	A/µs
		T2+ G-	-	50	A/µs
		T2- G-	-	50	A/µs
		T2- G+	-	10	A/µs
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	°C
T_j	Operating junction temperature		-	125	°C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.		UNIT
		BT136-			...	...F	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A					
		T2+ G+	-	5	35	25	mA
		T2+ G-	-	8	35	25	mA
		T2- G-	-	11	35	25	mA
		T2- G+	-	30	70	70	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
		T2+ G+	-	7	20	20	mA
		T2+ G-	-	16	30	30	mA
		T2- G-	-	5	20	20	mA
		T2- G+	-	7	30	30	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70		V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5		V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-		V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5		mA

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.		TYP.	MAX.	UNIT
		BT136-	...	...F			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	100	50	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 °C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	2	-	µs

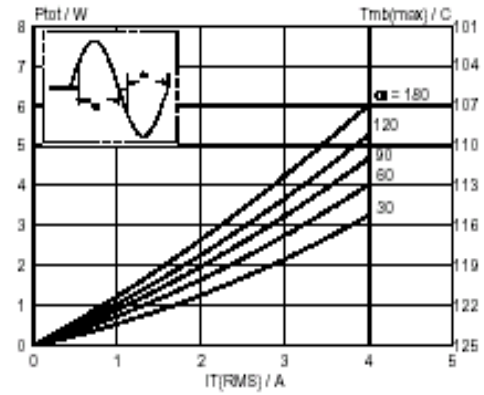


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

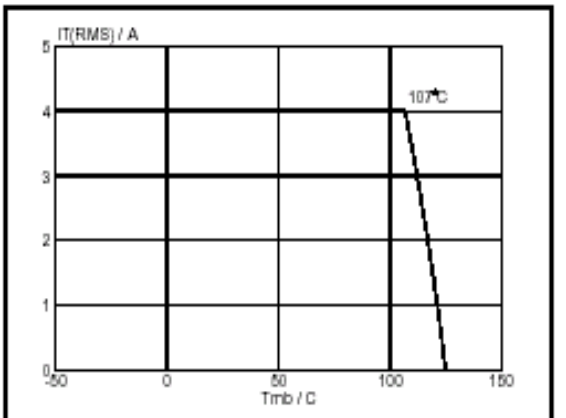


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

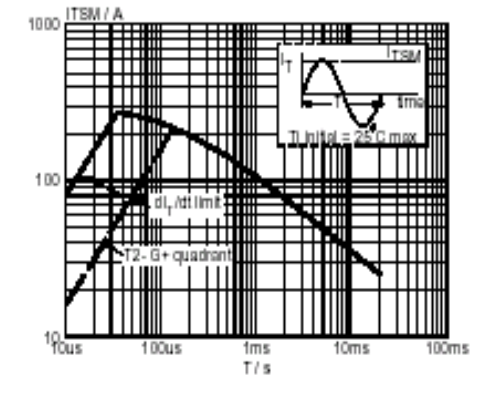


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

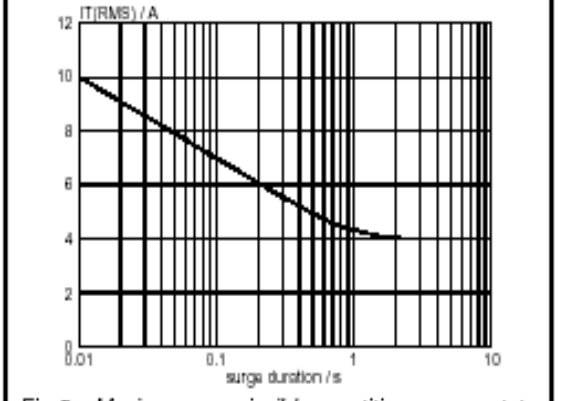


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.

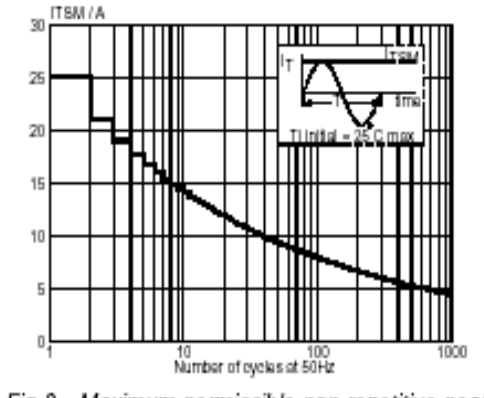


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

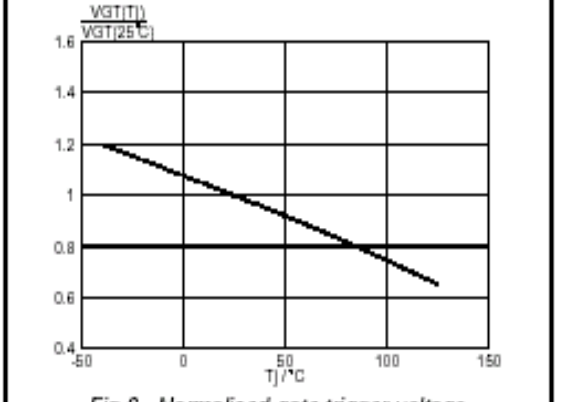


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

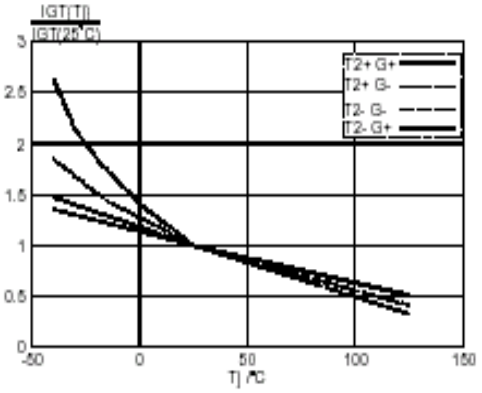


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

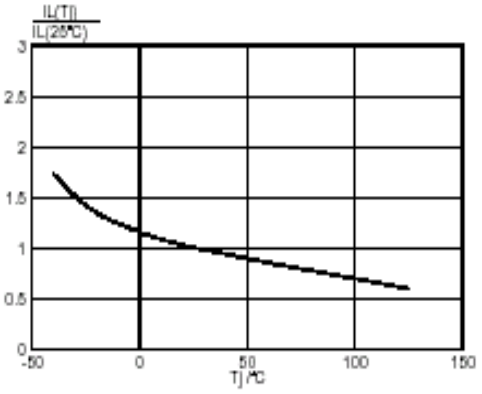


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

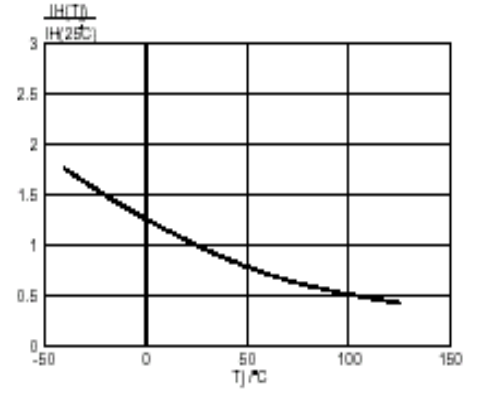


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

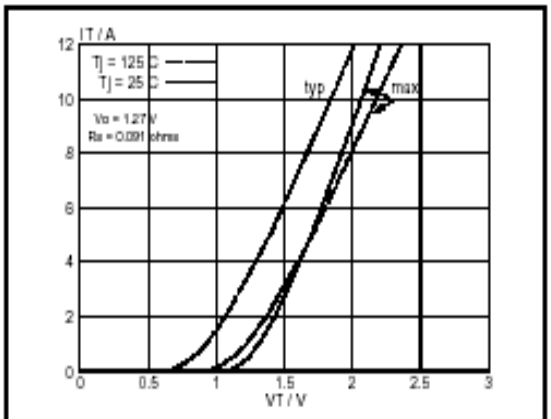


Fig.10. Typical and maximum on-state characteristic.

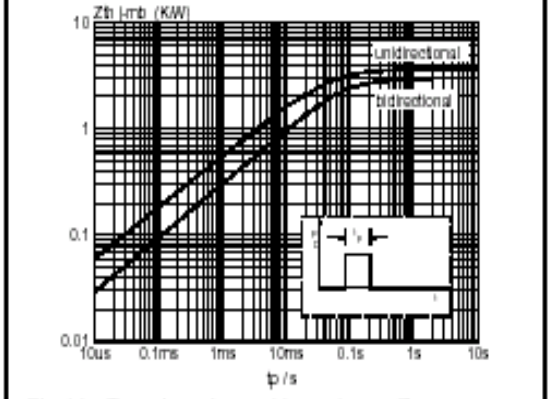


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

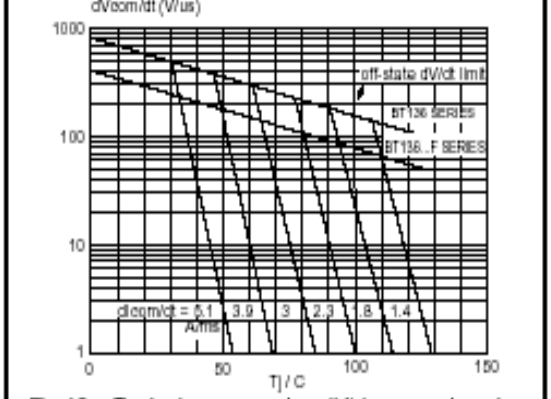


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.