

Description

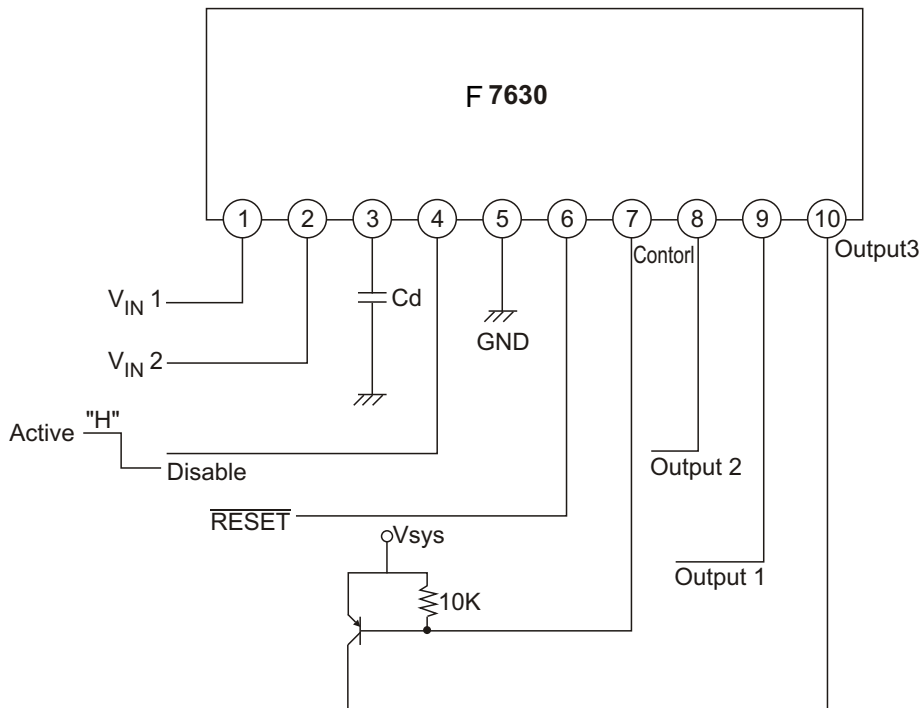
The F7630 is a multi-output positive voltage regulator, designed to provide fixed precision output voltages of 5.1V, 8V at current up to 0.5A and 12V at current up to 1A with external PNP transistor.

An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated value. Output2 & 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection, and thermal shutdown.

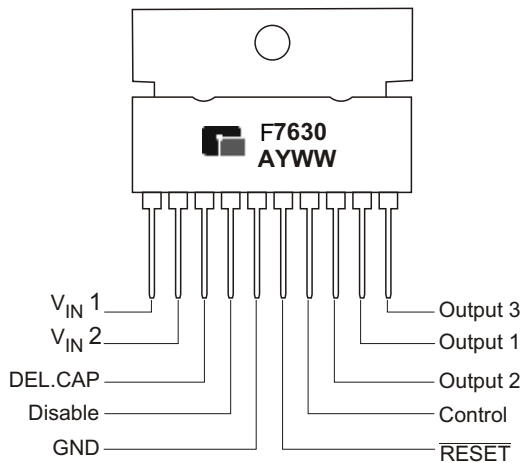
Features

- ◆ Output Currents up to 0.5A (output1 & 2)
- ◆ Output Current up to 1A with External Transistor (output3)
- ◆ Fixed Precision Output 1 voltage $5.1V \pm 2\%$
- ◆ Fixed Precision Output 2 voltage $8V \pm 2\%$
- ◆ Control Signal Generator for Output 3 voltage ($12V \pm 2\%$)
- ◆ Reset Facility for Output Voltage1
- ◆ Output 2,3 with Disable by TTL Input
- ◆ Current Limit Protection at Each Output
- ◆ Thermal Shut Down

TYPICAL APPLICATION



◆ MARKING INFORMATION & PIN CONFIGURATIONS (TOP VIEW)



A = Assembly Location
 Y = Year
 WW = Work Week

◆ ORDERING INFORMATION

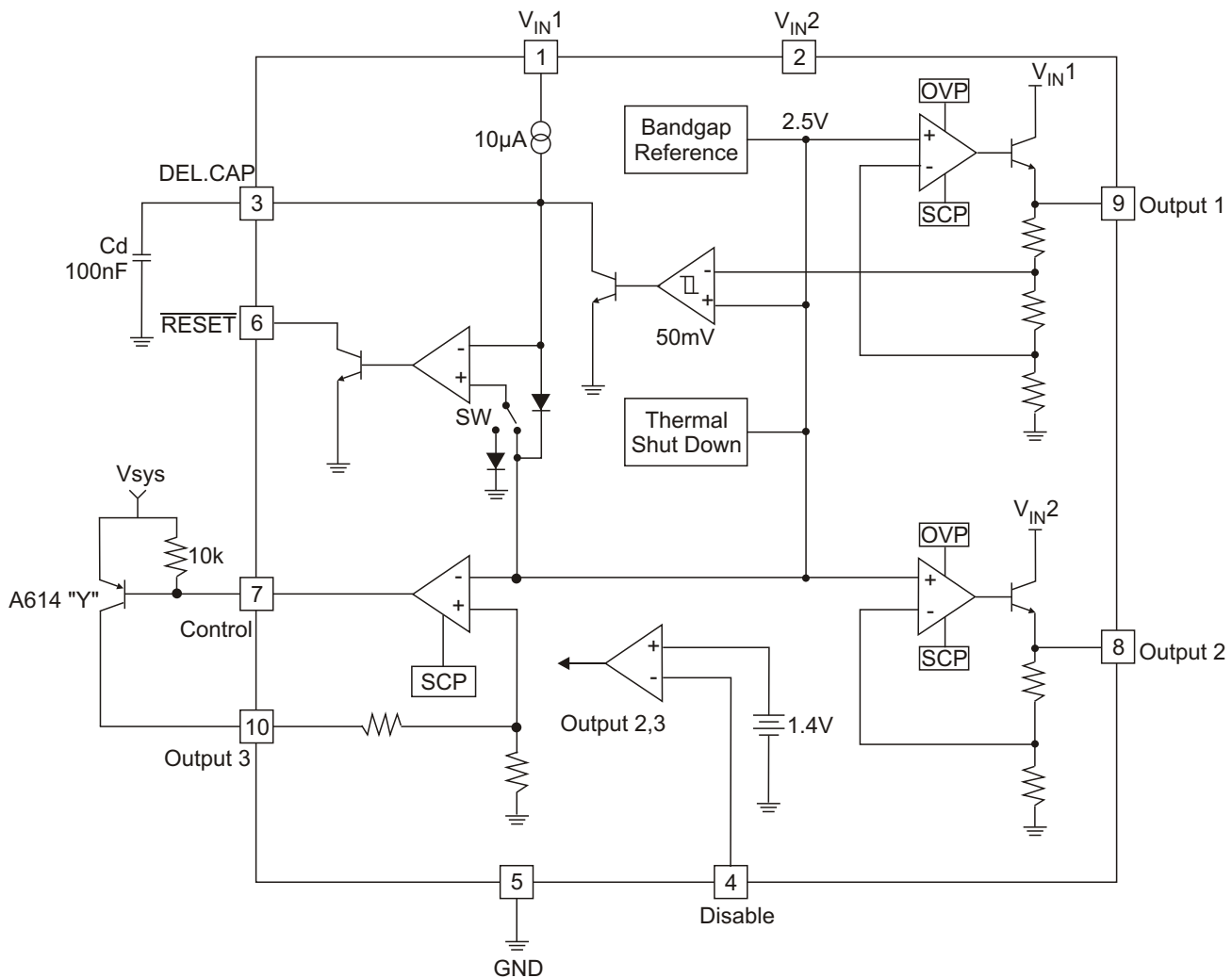
Ordering Number	Package	Shipping
F7630SIP10T	10- SIP H/ S	20 Units/ Tube

* For detail Ordering Number identification, please see last page.

◆ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS	REMARK
DC Input Voltage	V_{IN}	20	V	-
Disable Input Voltage	V_C	20	V	-
Output Current	I_O	0.5	A	-
Power Dissipation	P_D	1.5	W	No Heatsink
Junction Temperature	T_J	+150	°C	-
Operating Temperature	T_{opr}	0 ~ +125	°C	-

◆ INTERNAL BLOCK DIAGRAM



◆ ELECTRICAL CHARACTERISTICS

(Refer to test circuit $V_{IN1}=7.5V$, $V_{IN2}=10.5V$, $T_J=25^\circ C$, unless otherwise specified)

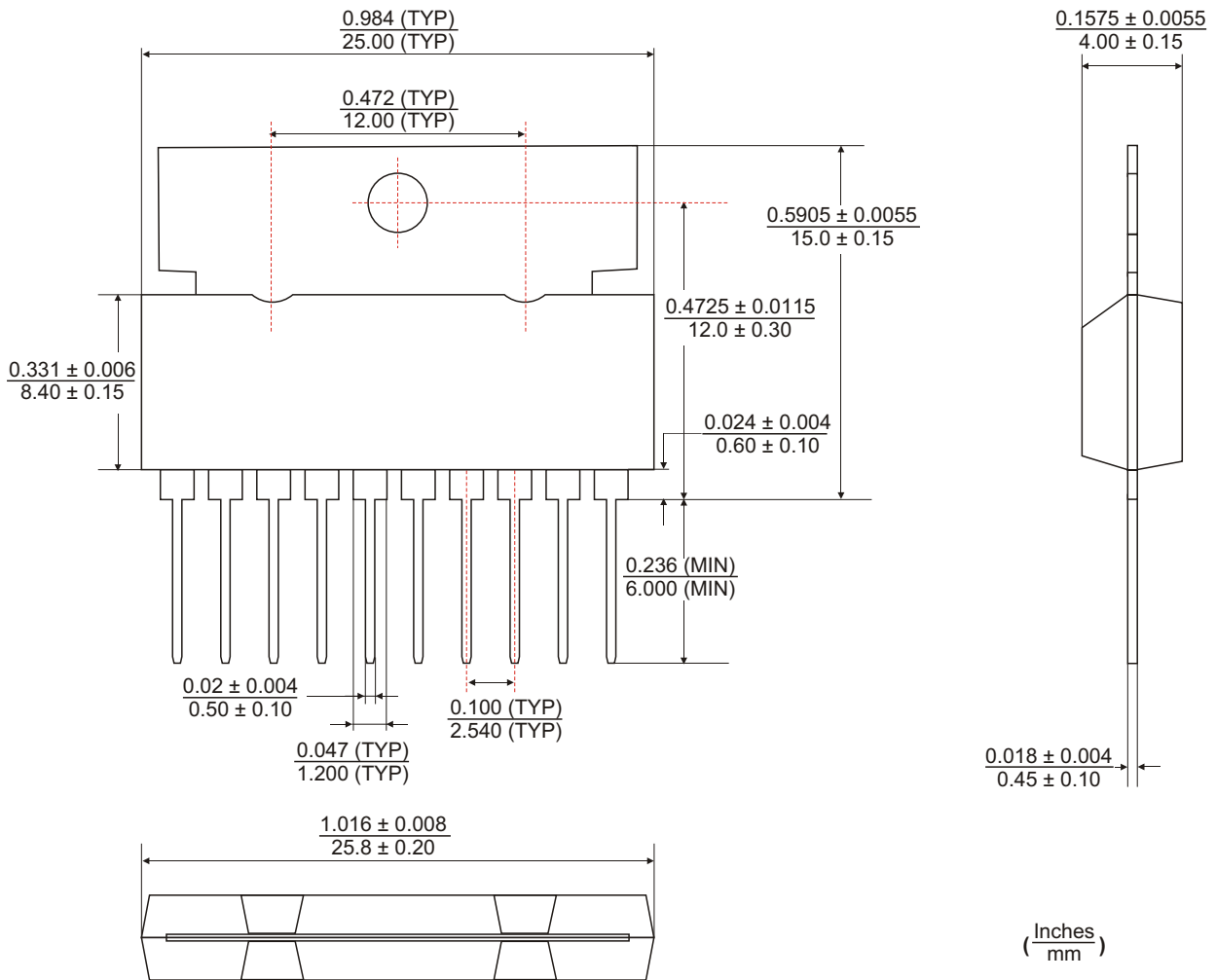
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage 1	V_{O1}	$I_{O1}=10mA$, $7.5V < V_{IN1} < 14V$ $5mA < I_{O1} < 500mA$	5.0 4.9	5.1 5.1	5.2 5.3	V
Output Voltage 2	V_{O2}	$I_{O2}=10mA$, $10.5V < V_{IN2} < 18V$ $5mA < I_{O2} < 500mA$	7.84 7.7	8 8	8.16 8.3	V
Dropout Output Voltage 1,2	$V_{d1,2}$	$I_{O1,2}=500mA$,	-	-	2.5	V
Line Regulation 1,2	$V_{O1,2}$	$7.5V < V_{IN1} < 14V$ $10.5V < V_{IN2} < 18V$ $I_{O1,2}=200mA$	-	-	50 80	mV
Load Regulation 1, 2	$V_{O1,2}$	$5mA < I_{O1} < 500mA$ $5mA < I_{O2} < 500mA$	-	0.1	100 160	mV
Output Voltage 3	V_{O3}	$V_{sys}=13V$, $I_{O3}=100mA$	11.7	12	12.3	V
Line Regulation 3	V_{O3}	$13V < V_{IN3} < 18V$ $I_{O3}=100mA$	-	-	120	mV
Load Regulation 3	V_{O3}	$5mA < I_{O3} < 1A$	-	-	250	mV
Reset Pulse Delay	Trd	$C_d=100nF$, Note 1	-	25	-	ms
Saturation Voltage in Reset Condition	VrL	$I_6=5mA$	-	-	0.4	V
Leakage Current Pin 6	IrH	$V_6=10V$	-	-	10	μA
Output Voltage Thermal Drift	STt	$0^\circ C < T_J < +125^\circ C$, Note 2	-	100	-	ppm/ $^\circ C$
Short Circuit Output Current	Isc 1,2	$V_{IN1}=7.5V$, $V_{IN2}=10.5V$	-	-	1.6	A
Disable Voltage High	VdisH	Output 2 Active	2.0	-	-	V
Disable Voltage Low	VdisL	Output 2 Disabled	-	-	0.8	V
Disable Bias Current	Idis	$0V < V_{dis} < 7V$	-100	-	2	μA
Junction Temperature for TSD	Tttd	Note 2	-	145	-	$^\circ C$
Quiescent Current	Iq	$I_{O1}=10mA$, Output2 Disabled	-	-	2	mA
Reset Threshold Voltage	Vr	$K=V_{O1}$	K -0.4	K -0.25	K -0.1	V
Reset Threshold Hysteresis	Vrth	Note 1	20	50	100	mA

Notes:

1. To check the reset circuit, the reset output is low to discharge the delay capacitor(=Cd). if it's less than $V_{O1}-0.25V$. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source($10\mu A$) if it's more than $V_{O1}-0.2V$. The equations of delay time is same as below. $Trd = (Cd \times 2.5) / 10\mu A$

2. These parameters, although guaranteed, are not 100% tested in production.

◆ 10-SIP H/S PACKAGE OUTLINE DIMENSIONS



◆ ORDERING NUMBER

