FMTS06N20ED 6.5A 20V Dual Die N-Channel ESD Protected Enhancement-Mode MOSFET

M-MOS Semiconductor Sdn. Bhd.

20V Dual N-Channel Enhancement-Mode MOSFET

V_{DS}= 20V **I_D= 6.5V** **ESD Protected : 2000V**
$R_{DS(ON)}$, V_{gs}@2.5V, I_{ds}@5.5A = 32mΩ
$R_{DS(ON)}$, V_{gs}@4.5V, I_{ds}@6.5A = 24mΩ

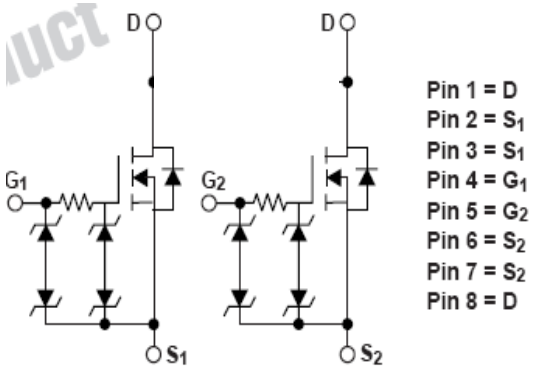
Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
Specially Designed for Li ion battery packs use
Designed for battery switch applications
Battery Swicth, ESD protected

TSSOP-08

Top View

Internal Schematic Diagram



N-Channel MOSFET

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current		I_D	6.5	A
Pulsed Drain Current [1]		I_{DM}	25	
Maximum Power Dissipation	T_A = 25°C	P_D	1.5	W
	T_A = 75°C		0.96	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		$R_{\theta JA}$	50	

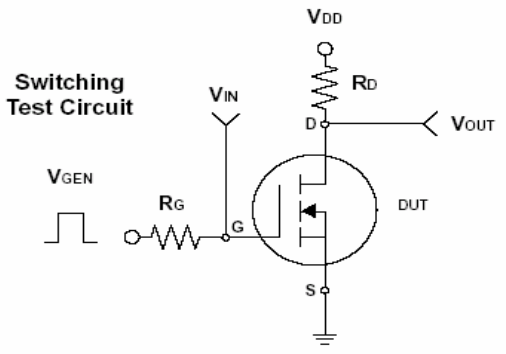
Note: 1. Repetitive Rating: Pulse width limited by the Maximum junction temperation
2. 1-in^2 2oz Cu PCB board
3. Guaranteed by design; not subject to production testing

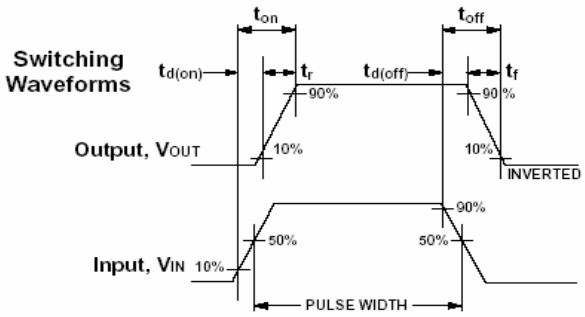
Dual N-Channel Enhancement-Mode MOSFET

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	25	-	-	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 2.5V, I_D = 5.5A		26.0	32.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 6.5A		20.0	24.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = 250uA	0.6	0.8	1	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0V			±10	uA
Forward Transconductance	g_{fs}	V_{DS} = 10V, I_D = 6.5A				S
Dynamic [3)]						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 6A V_{GS} = 4.5V		4.33		nC
Gate-Source Charge	Q_{gs}			1.05		
Gate-Drain Charge	Q_{gd}			2.49		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 1A, V_{GEN} = 4.5V R_G = 6Ω		354.67		ns
Turn-On Rise Time	t_r			873.33		
Turn-Off Delay Time	$t_{d(off)}$			3606.7		
Turn-Off Fall Time	t_f			2006.7		
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V f = 1.0 MHz		561.4		pF
Output Capacitance	C_{oss}			102		
Reverse Transfer Capacitance	C_{rss}			62.5		
Source-Drain Diode						
Max. Diode Forward Current	I_S				1.7	A
Diode Forward Voltage	V_{SD}	I_S = 1.5A, V_{GS} = 0V			1.2	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%





30V N-Channel Enhancement-Mode MOSFET

V_{DS}= 30V

$R_{DS(ON)}$, Vgs@10V, Ids@5.8A = 28mΩ

$R_{DS(ON)}$, Vgs@4.5V, Ids@5A = 33mΩ

$R_{DS(ON)}$, Vgs@2.5V, Ids@5A = 52mΩ

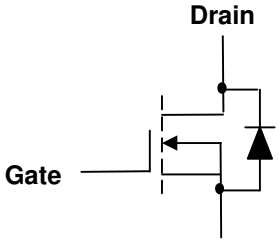
Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
Fully Characterized Avalanche Voltage and Current
Suitable for use as a load switch or in PWM application

SOT-23

Top View

Internal Schematic Diagram



N-Channel MOSFET

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current		I_D	6	A
Pulsed Drain Current 1)		I_{DM}	30	
Maximum Power Dissipation	T_A = 25°C	P_D	2.0	W
	T_A = 75°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) 2)		$R_{\theta JA}$	62.5	°C/W

Note: 1. Maximum DC current limited by the package
2. 1-in^2 2oz Cu PCB board

N-Channel Enhancement-Mode MOSFET

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	30	-	-	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 2.5V, I_D = 5A		43	52	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 5A		27	33	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 5.8A		24	28	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = 250uA	0.6	0.8		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V			1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			± 100	nA
Gate Resistance	Rg			0.6		Ω
Forward Transconductance	g_{fs}	V_{DS} = 15V, I_D = 15A	7	13		S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 6A V_{GS} = 6.9V		5		nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V, R_L = 2.2Ω I_D = 1A, V_{GEN} = 10V R_G = 3Ω		8.1		ns
Turn-On Rise Time	t_r			9.95		
Turn-Off Delay Time	$t_{d(off)}$			21.85		
Turn-Off Fall Time	t_f			5.35		
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V f = 1.0 MHz		562		pF
Output Capacitance	C_{oss}			106		
Reverse Transfer Capacitance	C_{rss}			75		
Source-Drain Diode						
Max. Diode Forward Current	I_S				1.7	A
Diode Forward Voltage	V_{SD}	I_S = 1A, V_{GS} = 0V			1.2	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%